A Novel AHB Based SDRAM Memory Controller

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ABSTRACT
This paper describes design of the memory controller which is compatible with Advanced High-performance Bus (AHB), which is a new generation of AMBA bus. The AHB is mainly meant for high-performance and high clock frequency system modules. The Memory Controller using FIFO provides command signals for memory refresh, read & write operations and initialization of SDRAM. Our work will focus on SDRAM Controller that is located between the SDRAM and AHB interface. The Controller simplifies the SDRAM command interface to standard system read/write interface and also optimizes the access time of read/write cycle.

Index Terms – SDRAM Controller, Read/Write Data path, AHB BUS

INTRODUCTION
ASIC implementation of DDR SDRAM Memory Controller is used in previous technique, but in which DDR memories have a disadvantage of a complex interface protocol. This protocol may require several memory cycle to complete one Write/Read operation based on the state of the memory. Throughput is decreased, Speed is less and performance is also low. By using VHDL Length of the program increased. The ASIC Design go through steps are Design entry, Analysis Technology Optimization and Floor planning, Design verification, layout. The Design challenges are becoming complex.

A NOVEL AHB Based SDRAM Memory Controller is used in proposed solution to re-architect the memory controller by embedding few FIFO’s in the data path of the memory controller. The FIFO’s are flip-flop based memories which are very small in size compared to the DDR so that the area overhead is not huge. Speed increases and performance is more. Our target is to reduce approx 90% of latency by using verilog HDL length of the program decreased.

In this paper is organized as follows:
DDR SDRAM Memory controller in section II AHB Based SDRAM Memory Controller in section III. The simulation results are presented in Section IV. Concluding remarks are made in Section V.

II. DDR SDRAM MEMORY CONTROLLER:

FIG.1 DDR SDRAM Controller System

The SDRAM controller, located between the SDRAM and the bus master minimizes the effort to deal with the SDRAM memory by providing a simple system to interact with the bus master. In this era of fast processors, there is a requirement for faster and bigger memories. But today the speed of fetching data from memories is not able to match up with speed of processors. So there is the need for a fast memory controller. The responsibility of the controller is to match the speeds of the processor on one side and memory on the other so that the communication can take place seamlessly. Here we have built a memory controller which is specifically targeted for SDRAM.

III. ADVANCED HIGH PERFORMANCE BUS (AHB)

AHB is a new generation of AMBA bus which is intended to address the requirements of high-performance synthesizable designs. It is a high-performance system bus that supports multiple bus...
masters and provides high-bandwidth operation. AHB is for high clock frequency system modules. It acts as the high-performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripherals. The motivation towards this project is as follows. To obtain fast and effective communication in modern large memory system with different data write and read operation of controller. To reduce the time delay of controller. To increase the high performance of controller using AHB bus. To make Controller is reconfigurable and scalable. The objective of this is to design a controller that can be used to implement both write and read operation with SDRAM controller based on read FIFO And it also can be used to reduce time delay of controller, to improve the high performance using AMBA AHB bus. AMBA AHB implements required for high-performance, high clock frequency system including: burst transfers Pipelined operation Multiple bus masters split transactions, wider data bus configurations (64/128 bits). The controller is expected to synchronize data transfer between the processor and memory. To achieve this, the controller has to accept the requests from the processor side and convert them to a form suitable to the memory and execute the requests.

The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called 0 and 1.

The advantage of DRAM is its structural simplicity that is only one transistor and a capacitor is required per bit, compared to four or six transistors in SRAM. In DRAM devices, large numbers of DRAM cells are grouped together to form DRAM array structures. Above figure illustrates a single bank of DRAM storage cells where a row address is sent to the row decoder, and the row decoder selects one row of cells. row of cells is formed from one or more word lines that are driven concurrently to activate one cell on each one of thousands of bit lines. There may be hundreds of cells connected to the same bit line, but only one cell will place its stored charge from its storage capacitor on the bit line at any one time. The resulting voltage on the bit line is then resolved into a digital value by a sense amplifier.

Since the processor is faster than the memory, it is illogical to make the processor wait till each command is executed for it to give the next command. So the controller has to have some kind of storage as given in figure above, so that it can buffer multiple requests from the AHB slave interface while the processor continues with other work. Dynamic random-access memory (DRAM) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated.
and when the accessing operation is done, the entire row address present in the row buffer is copied back to the SDRAM which is called as precharge. Precharge is done when there is any next operation has to be taken place and when the requested address is not matching with that of the address present in the row.

IV. SIMULATION RESULTS
FIFOing and burst-mode-data transfer. The testing results shows 91.66% of reduced delay with FIFOing when compared to the latency produced with out FIFOing, which is nothing but the in-built memory used within the SDRAM controller to improve its performance.

V. CONCLUSION
An AHB interfaced high-performance SDRAM Controller has been proposed, verified and evaluated we find this SDRAM controller has high performance by taking good use of the features of SDRAM architecture and utilizing the well-known techniques such as data FIFOing and burst-mode-data transfer. The testing results shows 91.66% of reduced delay with FIFOing when compared to the latency produced with FIFOing t, which is nothing but the in-built memory used within the SDRAM controller to improve its performance.

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