

Sareka Jeevane Dowrla<sup>1</sup>, K. Jhansi Rani<sup>2</sup>, <sup>1</sup>Project Associate, department of ECE, JNTUK, UCEK Kakinada A.P.

<sup>2</sup> Assistant Professor, department of ECE, JNTUK, UCEK Kakinada A.P.
<sup>1</sup> sareka.dowrla@gmail.com,<sup>2</sup> jhansikaka@gmail.com

### Abstract:

In this Paper, Digital Modulators is designed and Implemented using XILINX ISE Tool based on Very Large Scale Integration (VLSI). This is majorly to implement and obtain digitalize signals in softwaredefined radio (SDR) for signal power. SDR is a very widespread solution, whose modulation / demodulation methodology consists in programming the software in a dedicated programmable logic device (FPGA). This results in a high degree of versatility in the equipment because the same physical hardware can be used to implement different digital modulators / demodulators. In this context, Field-programmable gate-arrays (FPGA's) are the best solution, due to their best performance. Using XILINX software tools, the digital modulators schematic and simulations are designed and are presented, which helps to obtain accurate design constraints. As part of this we have integrated into Fieldprogrammable gate-array (FPGA) with the help of VERILOG Hardware Description Language (net-list). Here by using Spartan 3E the implementation is done and the results are observed.

Keywords-Digital Modulation, FPGA, VLSI, Xilinx

# I. INTRODUCTION

In general communication modulation is "the process of varying one or more properties of a periodic waveform i.e., the carrier-signal, for transmitting a modulating signal that contains information".

Modulation of a sine waveform is used to transform a baseband message signal into a pass band signal. A device that performs modulation is known as a modulator. A device that performs the inverse operation of modulation is known as a demodulator. A device that performs operations as modulator and demodulator is known as modem. The digital modulators major work is to transfer a digital bit stream over an analog band pass channel, for example over the wireless network (where a limit of band pass filter ranges in frequency is between 150 and 3400 Hz), or over a limited radio frequency band.

Digital modulation facilitate frequency division multiplexing (FDM), where several low pass information signals are transferred simultaneously over the same shared physical medium, using separate pass band channels (several different carrier frequencies). And the line coding, is to transfer a digital bit stream over a base band channel, typically a non-filtered copper wire such as a serial bus or a wired local area network as it is one of the aim of digital modulators.

The aim of digital modulation methods is to transfer a narrow band digital signal, in this scheme, as a bit stream over another digital transmission system.

Despite simple transmitter and receiver architecture of Digital modulators and its modulation technique is still commonly used in wireless communication such as WPAN (Wireless Personal Area Network). Amplitude shift keying (ASK) is data transfer technique with different amplitude of carrier frequency. As it is sensitive to propagate the channel variation, thus it is has been widely used in lowpower wireless transceiver for system simplicity.

For low power consumption, wireless communication systems exist in implantable medical devices, ingestible capsule endoscopy and multichannel neural recording. The ASK modulation/demodulation scheme, for both RF-band and baseband transceiver, was presented. This design is realized on future mobile memory I/O interface for energy efficient. However, BPSK is as well as showing better Bit Error Rate (BER) compared to BASK. In this work, it was shown that the need for a depressed decision threshold to optimally detect the received signal.



FIGURE-1: SCHEMATIC DIAGRAM FOR SOFTWARE-DEFINED RADIO TRANSMITTER

These digital modulation techniques were implemented on FPGA device. Simulation results consist of bit error rate of digital signals of modulators, source consumption of BASK, BFSK, BPSK and QAM FPGA-based, bit rate of BASK and BPSK on Xilinx ISE suite complier using verilog language. Thus digital modulators were implemented on FPGA.

In addition to, bit error rate of BASK and BPSK modulation techniques was compared using Xilinx. In this paper, for BPSK and BASK modulation, FPGA based modulator is presented. Finally, simulation results are obtained.



# FIGURE-2: SCHEMATIC DIAGRAM FOR SOFTWARE-DEFINED RADIO RECIEVER

Where as BPSK, QPSK, 16-QAM and 64-QAM are the permitted modulation schemes. Our work includes multimode interleaver design with all possible modulation scheme permitted. The interleaver comprises of two blocks: address generator and interleaver memory. The former is FSM based and the later is implemented using internal memory of FPGA. The FSM based address generator operates at higher frequency and can provide better FPGA resource utilization. Use of internal memory always provides better results in terms of memory access time, power consumption and real estate occupancy of circuit board compared to external memory. Two approaches have been adopted to model the interleaver memory: using dedicated internal memory and using distributed internal memory. Comparative analysis between the two techniques in terms FPGA resource utilization and maximum operating frequency shows that

the former technique out performs the later except the use of dedicated internal memory. The estimated power consumption of both techniques is equal and found to be 56mW. In addition our approach supports on the fly computation of interleaver addresses.

The Digital Signal Processing and the Channel Coding Stages where implemented within a FPGA (Spartan 3 line, from Xilinx) to take advantage of the massive parallel computation power of these devices and to have the possibility to scale up to ASIC devices.

The aim of this paper is implementation of fully digital modulators that employ the minimum number of digital blocks suitable for educational purpose, software-defined radio systems and are integrable with the FPGA board using Spratan3E. Furthermore, the implemented FPGA designs can be used in a digital communication course to demonstrate digital-modulation techniques

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The paper is organized as follows. In Section 2, the overview of digital modulator structures are briefly presented. In Section 3, the building blocks design of the digital modulators implemented in an FPGA are given, with details. The verification of digital modulators through simulations and real-time results acquired from the implementation into the Spratan3E FPGA board are emphasized and evaluated in Section 4 & 5. Thus at last in Section 6, conclusion is given.

II. OVERVIEW OF DIGITAL MODULATORS STRUCTURE

### **Digital modulation methods**

The major techniques for digital modulation are based on keying:

- BPSK (binary phase-shift keying): a finite number of phases are used.
- BFSK (binary frequency-shift keying): a finite number of frequencies are used.

- BASK (binary amplitude-shift keying): a finite number of amplitudes are used.
- QAM (quadrature amplitude modulation): a finite number of at least two phases and at least two amplitudes are used.

In QAM, an in-phase signal and a quadrature phase signal are amplitude modulated with a finite number of amplitudes, and then added. Here a two-channel system, each channel using BASK. The resulting signal is equivalent to a combination of BPSK and BASK.

A unique pattern of binary bits have being assigned by digital modulators and each phase, frequency or amplitude encodes an equal number of bits and the specific phase, frequency or amplitude comprises the *symbol*.

Thus  $M=2^{N}$ , Here each symbol represents a message consisting of *N* bits. If the symbol rate (also known as the baud rate) is fs symbols/second (or baud), the data rate is Nfs bit/second.

In digital modulators, the constant carrier signal and modulated signal is considered, the modulation signal is often conveniently represented on a constellation diagram, by representing the amplitude of the as I signal on the xaxis, and the amplitude of the Q signal on the y-axis, for each and every symbol.

### **Principles operation of modulators**

Sometimes the digital modulators are often generated and detected using the QAM principles. The thus I and Q signals can be combined into signal I+jQ, here *j* is the imaginary unit finally it is called equivalent low pass signal of the real-valued modulated signal and thus it is also called RF signal.

The procedure used to transmit the signal by the modulator:

- 1. Group the incoming data bits into code words, one for each symbol that will be transmitted.
- 2. Map the code words to attributes.
- 3. Adapt pulse shaping or some other filtering to limit the bandwidth and form the spectrum of the signals.
- 4. Perform digital to analog conversion of I and Q signals.
- 5. Generate a high frequency sine carrier waveform.

6. Amplification and analog band pass filtering to avoid harmonic distortion and periodic spectrum

At the receiver side, the demodulator typically performs:

1. Band-pass filtering.

2. Automatic gain control.

3. Frequency-shifting of the RF signal to the equivalent baseband I and Q signals, by multiplying the RF signal with a local oscillator sine wave and cosine wave frequency (see the super heterodyne receiver principle).

4. Sampling and analog-to-digital conversion (ADC).

5. Equalization filtering.

6. Detection of the amplitudes of the I and Q signals, of IF signal.

7. Quantization of the digital signals to the nearest allowed symbol values.

8. Mapping of the quantized amplitudes, frequencies or phases to code words (bit groups).

9. Parallel-to-serial conversion of the code words into a bit stream.

10. Pass the resultant bit stream on for further processing such as removal of any error-correcting codes.

All digital communication systems, the combination of the modulator and demodulator simultaneously are performed. Digital modulation schemes are possible because the transmitter-receiver pair have prior knowledge of how data is encoded and represented in the communications system. In all digital communication systems, the modulator and demodulator that consists of the transmitter and the receiver are structured so that they perform inverse operations.

Non-coherent modulation methods do not require a receiver reference clock signal that is phase synchronized with the sender carrier wave. In this case, modulation symbols are asynchronously transferred and an opposite is known as coherent modulation.

# III. INTERLEAVING SPEACIFICATIONS OF DIGITAL MODULATIONS

To design the modulators in hardware this specification is used.

Here, Ncpc is the no. of coded bits per sub-carrier, Ncbps is the no. of coded bits per allocated sub-channels, S is a parameter defined as  $s=max\{1, Ncpc/2\}$ .

## IV. HARDWARE MODEL OF INTERLEAVER

The proposed hardware model of interleaver consists of two sections: address generator and interleaver memory. In case of BPSK and QPSK (with s = 1) the increments are linear having value 3 and 6 space respectively. 16-QAM and 64-QAM have nonlinear increments e.g. 13, 11 and 20, 17, 17 space respectively. It contains three multiplexers (muxs) .mux-1 and mux-2 implements the unequal increments required in 16-QAM and 64-QAM whereas mux-3 routes the outputs received from mux-1 and mux-2 along with equal increments of BPSK and QPSK.



Fig: state diagram of digital modulators

The FSM enters into the first state (SF) with clr = 1. Based on the value in mod\_typ it makes transition to one of the four possible next states (SMT0, SMT1, SMT2 or SMT3). Each state in this level represents one of the possible modulation schemes.

Based on the value of the accumulator the next transition FSM state level is performed. When the FSM at this level reaches to the terminal value of that iteration (e.g.45 in SMT0), it makes transition to a state (e.g. S000) in which it loads the accumulator with the initial value (e.g. preset=1) of the next iteration.

This process continues till all the interleaver addresses are generated for the selected mod\_typ. If no changes take place in the values of mod\_typ, the FSM will follow the same route of transition and the same set of interleaver addresses will be continually be generated.

Any change in mod\_typ value causes the interleaver to follow a different path. To facilitate the address generator with on the fly address computation feature, we have made the circuit to respond to clr input followed by mod\_typ inputs at any stage of the FSM.

Thus by clr=1 it returns to SF state irrespective of its current position and there after transits to the desired states in response of new value in mod\_typ.

| Modulation<br>Scheme | Ncpc | S | Ncbps | no. of rows in<br>interleaver<br>memory |
|----------------------|------|---|-------|---|
| BPSK                 | 1    | 1 | 48    | 3                                       |
| QPSK                 | 2    | 1 | 96    | 6                                       |
| 16-QAM               | 4    | 2 | 192   | 12                                      |
| 64-QAM               | 6    | 3 | 288   | 18                                      |

### V. WORK DONE & RESULTS

Simulation procedure:

The design parameters used for simulation is 16-bit accumulator. This accumulator generates 16-bit digital sine wave with required frequency and phase respectively. And serial binary sequence is given, eg: 1110111...10. The input carrier signal was sinusoidal wave. The output modulated signal was digital signal. Thus, the simulation outputs of digital modulator is observed.

Simulation result 1:



Fig: output simulation block diagram of digital modulator

Simulation result 2:





Simulation result 3:



Fig: simulation output of digital modulator in p-n sequence

# VI. CONCLUSION

This paper briefly describes the digital modulators based on FPGA. And the design method of FPGA using Xilinx for simulation and hardware by using interleaving memory is analyzed in detail. Finally, an improved scheme is proposed. The implemented FPGA designs are suitable for realization of the digital modulation. By this method reducing number of blocks in digital modulation to gain ability and to integrate the modules in respective FPGA board is performed. User controllability of input signal frequency and obtained constant amplitude and phase values. But yet still need to overcome for generating the constant frequency value.

### REFERENCE

- [1] Design and performance analysis of a high speed AWGN communication channel emulator - Ghazel, Boutillon, et al. - 2001.
- [2] Http://www.ece.nus.edu.sg/stfpage/eleak/pdf/soia04.p df.
- [3] Digital modulation in FPGAs Xilinx using system generator (ASK, BPSK, FSK, OOK, QPSK) by diego Orlando 13 april 2007.
- [4] Http://mobiledevdesign.com/hardware\_news/radio\_err or control\_coding.Aqib.
- [5] Modulation schemes for digital modulators of class D amplifiers and of switched-mode DC-DC converter, Victor. Adrian.
- [6] Digital Modulation in FPGAs Xilinx using system generator (ASK, BPSK, FSK, OOK, QPSK) by Diego Orlando.
- [7] http://www.innovative-dsp.com/