E-IHRB Decoder Architectures for Non-Binary LDPC Codes
Kalyani Madamsetti 1 M.Tech Student (ECE), 2SUSEELA.M Assistant Professor (ECE), GDMM College Of Engineering And Technology,Nandigama. kalyani.madamsetty@gmail.com

Abstract— In the information theory, the non-binary low density parity check (NB-LDPC) code is a linear error correcting code, a method of transmitting message over a noisy transmission channel. LDPC codes are capacity-approaching codes, which means that practical constructions exist that allow the noise threshold to be set very close to the theoretical maximum for a symmetric memory less channel. Using iterative belief propagation techniques, NB-LDPC codes can be decoded in time linear to their block length. Non-binary low-density parity-check codes can achieve higher performance than their binary counterparts. Recently, two algorithms were developed for decoding NB-LDPC codes: iterative hard reliability-based majority-logic decoding (IHRB-MLGD) and iterative soft reliability-based majority-logic decoding (ISRB-MLGD) has better performance-complexity tradeoffs than previous algorithms. This paper first proposes message-passing in such a way that we can reduce the memory consumption to a greater extent at the same time there should not be performance loss. By using enhanced iterative reliability-based majority-logic decoding algorithms we can achieve effective complexity-performance and noise free design. Compared to previous designs, our proposed decoders have at least tens of times lower complexity with moderate coding gain loss.

Index Terms— IHRB-MLGD, ISRB-MLGD, low-density parity-check (LDPC) codes, non-binary, modelsim, xilinx, VLSI.

I. INTRODUCTION
Communication is a process of transferring data from one person to other person involves a lot of coding during the programming of its mechanism and the probability of getting errors is ample. Some of the simple bit errors can be adjusted by interpreting the real bit sequence during communicative path is down line. Most of the arbitrarily problems can be solved randomly utilizing few of the important features original sequence of algorithm which yields to the. The most important feature for communication is to facilitate error free data transmission among digital or analog functioning signals along with amplification. Coding in communication system is basically categorized into four sections as

- Encryption: mainly used for security of data,
- data compression: used for data streaming and to reduce the space,
- Data translation: used to demonstrate the data for transmission of communication channels
- Error Control: identifies the errors and correct them as soon as possible.

For digital signals data represented as 0 and 1’s, so as to detect errors and analyzing the noise occurred while transmission as well as to correct those errors. In normal cables the error is due to the random motion and some deviation occurs when conduction is through various components like resistors, capacitors, inductors etc, which is known well known as thermal noise. This is one of the major sources of noise for cable communication system. If there are various sources of noise in wireless communication systems such as in mobile phones, disturbances are of other user signal noise interruption. The original signal is normally added with the noise signal at receiver input.

![Fig(a): Block Diagram of E-IHRB](image-url)
II. RELATED WORK
Non-binary low-density parity-check (NB-LDPC) codes can achieve better error-correcting performance than their binary counterparts at the cost of higher decoding complexity when the codeword length is moderate. The recently developed iterative reliability-based majority-logic NB-LDPC decoding has better performance-complexity tradeoffs than previous algorithms. This paper first proposes enhancement schemes to the iterative hard reliability-based majority-logic decoding (IHRB-MLGD). Compared to the IHRB algorithm, our enhanced (E)-IHRB algorithm can achieve significant coding gain with small hardware overhead. Then low-complexity partial-parallel NB-LDPC decoder architectures are developed based on these two algorithms. Many existing NB-LDPC code construction methods lead to quasi-cyclic or cyclic codes. Both types of codes are considered in our design.

III. PROPOSED WORK
In proposed system, we are sending messages in such a way that we can reduce the memory consumption to a greater extent at the same time there should not be performance loss. By using iterative reliability-based majority-logic decoding algorithms we can achieve effective complexity-performance and noise free design. By using shift message structure, we can concatenate memories with variable node units to enable efficient partial-parallel decoding for cyclic NB-LDPC codes. Compared to previous designs, our proposed decoders have at least tens of times lower complexity with moderate coding gain loss. In information theory, a non binary low-density parity-check (NB-LDPC) code is a linear error correcting code, a method of transmitting a message over a noisy transmission channel. LDPC codes are capacity-approaching codes which means that practical constructions exist that allow the noise threshold to be set very close to the theoretical maximum for a symmetric memoryless channel. The noise threshold defines an upper bound for the channel noise, up to which the probability of lost information can be made as small as desired. Using iterative belief propagation techniques, NB-LDPC codes can be decoded in time linear to their block length. Non-binary low-density parity-check codes can achieve higher performance than their binary counterparts. The random LDPC codes are generally outperform structured LDPC codes since they have better distance properties, particularly for long code lengths. Recently, two algorithms were developed for decoding NB-LDPC codes: iterative hard reliability-based majority-logic decoding (IHRB-MLGD) and iterative soft reliability-based majority-logic decoding (ISRB-MLGD) has better performance-complexity tradeoffs than previous algorithms. Recently, two algorithms were developed for decoding NB-LDPC codes: iterative hard reliability-based majority-logic decoding (IHRB-MLGD) and iterative soft reliability-based majority-logic decoding (ISRB-MLGD). In these algorithms, reliability messages are incorporated into majority-logic decoding and improved through an iterative process. Unlike previous BP-based algorithms, these two algorithms require only simple check sum computations over in the check node processing. Moreover, only one set of reliability messages need to be stored for the received symbols and the messages passed from a variable node to all connected check nodes are the same. Hence, the memory required for storing messages can be greatly reduced. As a result, these iterative reliability-based majority-logic decoding algorithms can achieve effective complexity-performance tradeoff. Compared to the ISRB algorithm, the IHRB algorithm updates reliability messages based on the hard decisions instead of probabilities of the received symbols. Hence, at the cost of moderate coding gain loss, the IHRB algorithm has much lower computation complexity and memory requirement than the ISRB algorithm. Nevertheless, mapping the IHRB algorithm directly to hardware implementation still leads to high complexity.

IV. SIMPLER DECODING
- We now describe an alternative decoding procedure that can be implemented very simply.
- It is a “local” decoding technique that tries to fill in erasures “one parity-check equation at a time.”
- We’ll compare its performance to that of optimal bit-wise decoding.
- Then, we’ll reformulate it as a “message-passing” decoding algorithm and apply it to LDPC codes.

V. MESSAGE-PASSING DECODING
The local decoding procedure can be described in terms of an iterative, “message-passing” algorithm in which all variable nodes and all check nodes in parallel iteratively pass messages along their adjacent edges. The values of the code bits are updated accordingly.

VI. SCOPE OF WORK
- Most of the LDPC in the market are a parameterizable intelligent property (IP) core with an efficient algorithm for decoding of one encoded sequence only.
- The cost for the LDPC are expensive for a specified design because of the patent issue.
• To realize on a field programmable gate array (FPGA) board is very demanding.

V. IMPLEMENTATION RESULTS

Results Analysis:

SIMULATION RESULT:
The below figures shows the simulation results of test cases applied to the DUT:

Simulation results for top module:

![Snapshot: Memory internal circuitry](image)

Schematic RESULTS from Xilinx:

Snap shot: Internal circuitry of block diagrams

![Snap shot: control circuit internal](image)

5.3 CONCLUSION:

In order to avoid the delay, we use the latest verification methodologies and technologies and accelerate the verification process. This thesis helps one to understand the complete design and verification flow. Designing & Verification is done by Verilog HDL using Modelsim and Xilinx Tools to get simulated and synthesized outputs.

Future Work:

This project used Verilog i.e., the technology used is direct test cases, for verification even though the coverage is 100% there may be some errors which cannot be shown so in order to overcome this the new technology of System verilog i.e. OVM and UVM. In the coming future the Frequency Synthesizer can be done by using OVM and UVM.

REFERENCES:


Mrs.M.SUSEELA is currently working as an assistant professor in ECE Department, GDMM college of engineering and technology, Nandigama, A.P, India. She received his M.Tech from BVC engineering college, Odalarevu, amalapuram. Her research interests in the area of Embedded Systems.

Ms.M.kalyani received her B.Tech degree from the department of Electronics and Communication Engineering, MIC College of technology (Affiliated to JNTU Kakinada), Kanchikacherla, A.P, INDIA. She is pursuing M.Tech in GDMM college of engineering and Technology (Affiliated to JNTU Kakinada), Nandigama, AP, India. Her current research interests are VLSI design.