A Logic Test to Minimize Test Data Volume By Single Cycle Access Structure

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Abstract: This research proposes an a logic test to minimize test data volume by single cycle access structure. It eliminates the peak power consumption problem of conventional shift-based scan chains and reduces the activity during shift and capture cycles. This leads to more realistic circuit behavior during stuck at and a tspeed tests. It enables the complete test to run at much higher frequencies equal or close to the one in functional mode. It will be shown, that a lesser number of test cycles can be achieved compared to other published solutions. The test cycle per net based on a simple test pattern generator algorithm without test pattern compression is below 1 for larger designs and is independent of the design size. Results are compared to other published solutions on ISCAS’89 net lists. The structure allows an additional on-chip debugging signal visibility for each register. The method is backward compatible to full scan designs and existing test pattern generators and simulators can be used with a minor enhancement. It is shown how to combine the proposed solution with built-in self test (BIST) and massive parallel scan chains.

Index Terms – At-speed testing, low-power testing, on-chip signal visibility, switching activity during test, test-time reduction.

1. INTRODUCTION

The Production test costs of chips become more and more dominant. The standard shift scan (SS) method is the most popular test implementation within the last decades. It has been tried to improve this approach in terms of test time, test data volume and test power by optimizing the scan pattern, using different scan chain structures, different scan support logic, or a combination of these modifications.

Automatic test pattern generation (ATPG) for sequential VLSI Circuit is an NP-complete problem with an exponential complexity. The complexity of combinatorial logic varies. Complex and hard to test logic needs to be stimulated and captured quite often but the pattern need to be shifted throughout the complete scan chain. One approach to reduce test time is to use parallel scan chains. This leads to a massive increase of parallel scan chain to reduce the length of the scan chains, for reduce test data volume, a built-in self test (BIST) mechanism is used.

The high peak power during shift leads to an excessive current due high switching activity, which can lead to a miss-classification of the circuit under test. The pattern reduction for at-speed tests is proposed by pomeranz by test compaction based on non-scan test sequences and the removal of the transfer sequences. None of the methods fundamentally solve the problem of high switching activity, a high number of test cycles and a slow global scan enable signal simultaneously.

Built-in self test (BIST) is a solution to reduce test data volume and can further on reduce the test access pins for the CUT dramatically. The Embedded logic test method is a well-established method. BIST
based on a RAS is examined by Yao. A new test implementation must therefore be usable in a BIST environment.

This paper presents a novel scan cell register for logic tests combined with a novel scan cell routing architecture. The structure allows a single cycle access (SCA) to individual register sets. This access scheme is fundamentally different to SS. It can be compared to a memory with a single cycle synchronous write and asynchronous read functionality, where as the remaining memory content registers does not change. Unlike with a certain number of shift cycles in shift–scan designs, the values can be read and written with one single cycle. The structure needs less test cycles to reach a certain or full coverage and the power consumption during tests is in the range of the one in functional mode. This allows higher test frequencies and leads to more realistic test conditions closer to the functional chip behavior during stuck–at and at–speed tests.

This paper is structured as follows. In Section II “SCAh – Structure with Hold Mode”, the single cycle access test structure is explained. The feasibility, area, test cycles, power consumption, and debugging capabilities of this solution is compared to alternative state of the art methods. In Section III, “SCA – Structure without Hold Mode” demonstrates further solutions to overcomes the area disadvantage of the Proposed Method. The Advantages of the SCAh – Structure and the lower area overhead of the SCA – structure are combined and presented in Section IV, “Gated SCA-Structure “,and V “Address Controlled BIST”, solutions which can be applied to today ‘s test requirements. The numbers in Section VI “Results”, demonstrate the advantage of the lower test cycles per net resulting from the proposed solutions.

II. SCAh – STRUCTURE WITH HOLD MODE

The Key Element of the single cycle access structure with hold mode (SCAh) is the signal cycle access register (FlipFlop, FF) with hold mode (SCAh –FF). It is based on a standard scan register (S-FF) and uses two more 2 – to -1 multiplexers. The new SCAh-FF can be seen in Fig 1.

The SCAh-FF has one more input and one more output compared to the standard shift register (S-FF). The inputs clock (clk), data_in(di), and scan_in (si) still exists. The scan-enable is now a 2 bit bus {se[0:1]}. An additional scan output pin (so) is added. The reset input and inverse output pins are not shown. The internal logic enables the register to run in one additional hold mode, where as the additional output multiplexer can by pass the register to directly drive the value of {si}. The resulting functionality is best explained by a truth table.

Table 1 : Truth Table of SCAh -FF

<table>
<thead>
<tr>
<th>Se[0:1]</th>
<th>do@clk</th>
<th>so</th>
<th>mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>di</td>
<td>si</td>
<td>functional</td>
</tr>
<tr>
<td>01</td>
<td>di</td>
<td>do</td>
<td>async, read</td>
</tr>
<tr>
<td>10</td>
<td>do, unchanged</td>
<td>si</td>
<td>hold</td>
</tr>
<tr>
<td>11</td>
<td>Si</td>
<td>do</td>
<td>sync, write/read</td>
</tr>
</tbody>
</table>

In functional mode ({se[0:1]} == “00”), the register captures {di} and {so} follows {si} (usually stable). In read mode {so} has the value of {do} so that {do} can be read out asynchronously. In the event of the relevant clock edge, the register captures {di}. In
hold mode, \{so\} follows \{si\}, and the register remains in the state \{do\}, capturing its own value. When \{se[0:1]\} == “11”, the registers captures \{si\} and \{so\} changes to the new value of \{do\} (sync.write/read mode).

The two major differences are, that the scan-in \{si\} is now connected to a dedicated scan-out\{so\} of the preceding register in the scan chain and register\{se[1]\} inputs on the same scan depth are connected to the same line --select \{ls\} signal, which is driven by a “1 out of N” decoder. SCAh –FF connected to the same line select signal are considered to be on one line. If \{add\} is 0, no line is selected. \{Se[0]\} of each SCAh –FF is connected to the global scan enable signal \{gse\}. The output of address decoder is connected to the \{se[1]\} pin of the registers on one particular line.

4. If a specific address is given at a relevant clock edge and \{gse\} is high, the scan-in values \{si\} are captured by the registers on the selected line (Synchronous Write) and Scan-out \{so\} is driven by the captured register value (read). This mode is called Synchronous write/Read.

In this rather extreme compact case, the page uses a global 1-out-of-31 address line decoder. A page selector \{Ps\} selects the individual page and drives the scan input bus signals and line select \{ls\} signals (AND-ed) only of this particular page. \{ps\} can be driven by a register which is set by a dedicated test control logic. If not selected, the page remains inactive to reduce activity.

Figure 2: SCAhS Connectivity

From this structure four different Kinds of cycle modes result.

1. When \{gse\} is low and \{add\} is 0, the design work in normal functional model.

2. If a specific address is given, the register values on the selected line are passed to the scan-out bus \{so\}. This mode is called asynchronous read mode.

3. When \{gse\} is high and \{add\} is 0 (no line selected), the design remain in hold mode and no register value changes during an clock edge.

4. If a specific address is given at a relevant clock edge and \{gse\} is high, the scan-in values \{si\} are captured by the registers on the selected line (Synchronous Write) and Scan-out \{so\} is driven by the captured register value (read). This mode is called Synchronous write/Read.

In this rather extreme compact case, the page uses a global 1-out-of-31 address line decoder. A page selector \{Ps\} selects the individual page and drives the scan input bus signals and line select \{ls\} signals (AND-ed) only of this particular page. \{ps\} can be driven by a register which is set by a dedicated test control logic. If not selected, the page remains inactive to reduce activity.

Figure 3: SCAh – Page, Global scan enable not shown.

The scan output buses of all pages \{so\} are bit-wise XOR-ed with the \{so\} of other pages to generate the global scan-out bus \{pso\}. If the page is inactive, the XOR-tree passes the value of previous pages unchanged since all \{so\} bits of an unselected page are “0”.

With the page organization, the relevant timing paths become clear. During a read, the registers are selected by the line-select signal and drive the scan-out bus \{so\} through a multiplexer chain of the succeeding registers and the page-scan-out bus \{pso\} through the XOR-tree. During a write, the scan-in bus \{si\} values are passed through the
AND-selector and the multiplexer chain of the trailing register to the registers of the selected line.

### III. SCA-STRUCTURE WITHOUT HOLD MODE

In order to reduce the area overhead of a SCAhS, a simpler SCA-FF is discussed. It adds only one 2-to-1 MUX to the standard S-FF (the truth table is shown in Table II. It only has one \{se\} input, which is connected to the individual line-select signal. The pin which is connected to the global enable signal in the SCAhS is removed, so that the complete global scan enable tree becomes obsolete. The SCA-structure (SCAS) connectivity and page organization equals the one of the SCAhS (see Figs. 2 and 3) without the global scan enable \{gse\}.

The SCAS basically has the advantages of a single cycle synchronous write and a single cycle synchronous read of a register line. The pSCAhS and the SCAS have in common, that a majority (pSCAhS) or all (SCAS) of the registers do not have a hold mode and automatically capture the new value if a write to a register line is done. This fact makes the TPG an extremely complex task. Therefore, the TCPN for the SCAS are purely based on random pattern generation and does not always reach 100% coverage.

<table>
<thead>
<tr>
<th>Sc</th>
<th>do</th>
<th>@clk</th>
<th>so</th>
<th>mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>di</td>
<td>si</td>
<td>si</td>
<td>Functional</td>
</tr>
<tr>
<td>1</td>
<td>si</td>
<td>do</td>
<td>do</td>
<td>Sync, write, async, read</td>
</tr>
</tbody>
</table>

### IV. Gated SCA –Structure

The gated SCAS (gSCAS), which has all the benefits of the SCAhs but only has the area overhead of the SCAS. The hold function of the SCAh-FF is missing in the SCA-FF. It is instead built into the gated clock tree of the gSCAS. The Scan Path reaches from the scan-in And-Selector over the SCA-FF Chain and is connected with the input of the XOR-tree. The individual line-select signals \{ls\} are connected with the \{se\} input of the SCA-FF in the relevant line. All SCA-FF on a line are clocked by a gated clock element (gcl). The gcl is driven by the clock and the line-select signal. The gated clock element can be enhanced, if a clock enable signal \{ce\} generated by combinatorial logic exists. The global scan enable signal is connected with each gcl, which is already the case in SS if gated clock element are used to propagate the clock during shift.

A problem in testing is the high test data volume for the ATE. This test amount is reduced by BIST implementations since SCAhS and gSCAS are backward compatible to shift scan implementations (by automatically incrementing the address during “shift”), existing BIST solutions can be used on them as well. An additional problem is the high number of test pins for testing. In this section a method is proposed to reduce the pin count of the test IOs on an address controlled SCAhS or gSCAS-BIST.
The principle idea of BIST is not to apply write values to the DUT by the tester but instead taking them from the scan-out values of the DUT internally. These deterministic pattern generated by the DUT are used with or without (de-)compression logic as the stimuli of the DUT itself. This BIST mechanism is used in the proposed structure. Only the address signals \{add\} are controlled to optimize the process. With an address controlled read the internal values of a particular line of the enabled pages are then propagated through the XOR tree to the scan output. The scan-out pattern can also be used as scan-in pattern and an address controlled write can be done.

The address controlled BIST structure is as follows. An on-chip test controller can be accessed by the ATE. The controller can enable and disable individual pages. It also controls the register mode (functional/capture, write, read and hold) by applying the right values to \{gse\}, \{psel\}, and \{add\}. The page scan-in data are taken from the scan-out data of the XOR tree be set by a shift register.

VI. RESULT:

Test compaction for at-speed testing is used in order to reduce the test application time. The algorithm in reduces switching activity during scan testing and simultaneous test time and power reduction. In the reduction of test application time using limited scan Operations The TCPN for any single cycle access structure as well as for the shift based structure will decrease with a higher SW. The number of input address bits of the address decoder is defined as ABIT.

![Simulation Result of Logic test single cycle access](image)

VII. CONCLUSION

A single cycle access structure is discussed. Various implementations with and without hold ode as well as gated and partial implementation methods are presented. The aspects feasibility, peak power consumption, switching activity during test, area, test cycles, at-speed testing and debugging features are compared. A guide is given how to select the best implementation. The best solution (gSCAS) is compared to RAS implementations and is superior to all known RAS solutions. If BIST is preferable due to limited chip IOs or partial scan implementation, an address controlled BIST is discussed.

The ATPG algorithms can be enhanced with the same methods SS implementations are optimized. Future work is related to algorithms for reducing the test cycles per net itself, register reordering, pattern optimization for activity reduction and de-/compression methods for BIST using the gSCAS.

REFERENCES


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