Wireless real time health monitoring system built with FPGA and RF networks
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Abstract
In recent Days, heart disease is a major concern in the health indicator for the elderly. Cardiovascular diseases are always the leading cause of death in many countries. Due to the rapid growth of elderly population in recent years, health monitoring systems have played a more important role in the early detection of heart attack and cardiovascular diseases. In this project, a real-time ECG monitoring system featuring HRV (Heart Rate Variability) analysis and wireless data transmission through radio frequency based on a System-on-Chip (SoC) development platform is proposed.

Modelsim Xilinx Edition (MXE) and Xilinx ISE will be used simulation and synthesis respectively. The Xilinx Chipscope tool will be used to test the FPGA inside results while the logic running on FPGA. The Xilinx Spartan 3E Family FPGA development board will be used for this project.

I. INTRODUCTION
At present, cardiovascular diseases have become a threat to human life and health for major diseases, and morbidity increases year by year. The prevalence rate of cardiovascular disease, morbidity and mortality upward trend continued, the death toll of about 40% of the number of deaths, therefore, focus on the prediction of cardiovascular disease diagnosis and prevention is an important significance.

II. Electrocardiogram
An electrocardiogram (EKG or ECG) is a test that checks for problems with the electrical activity of your heart. An EKG translates the heart's electrical activity into line tracings on paper. The spikes and dips in the line tracings are called waves. See a picture of the EKG components and intervals in figure 1. The heart is a muscular pump made up of four chambers. The two upper chambers are called atria, and the two lower chambers are called ventricles. A natural electrical system causes the heart muscle to contract and pump blood through the heart to the lungs and the rest of the body.

An electrocardiogram (EKG or ECG) is done to:
1) Check the heart's electrical activity.
2) Find the cause of unexplained chest pain, which could be caused by a heart attack, inflammation of the sac surrounding the heart (pericarditis), or angina.
3) Find the cause of symptoms of heart disease, such as shortness of breath, dizziness, fainting, or rapid, irregular heartbeats (palpitations).
4) Find out if the walls of the heart chambers are too thick (hypertrophied).
5) Check how well medicines are working and whether they are causing side effects that affect the heart.
6) Check how well mechanical devices that are implanted in the heart, such as pacemakers, are working to control a normal heartbeat.
7) Check the health of the heart when other diseases or conditions are present, such as high blood pressure, high cholesterol, cigarette smoking, diabetes, or a family history of early heart disease.

An electrocardiogram (EKG or ECG) is usually done by a health professional, and the resulting EKG is interpreted by a doctor, such as an internist, family medicine doctor, electro physiologist, cardiologist, anesthesiologist, or surgeon.

You may receive an EKG as part of a physical examination at your health professional's office or during a series of tests at a hospital or clinic. EKG equipment is often portable, so the test can be done almost anywhere. If you are in the hospital, your heart may be continuously monitored by an EKG system; this process is called telemetry.

During an EKG:
1) Areas on your arms, legs, and chest where small metal discs (electrodes) will be placed are cleaned and may be shaved to provide a clean, smooth surface to attach the electrode discs. A special EKG paste or small pads soaked in alcohol may be placed between the electrodes and your skin to improve conduction of the electrical impulses.

2) Several electrodes are attached to the skin on each arm and leg and on your chest. These are hooked to a machine that traces your heart activity onto a paper. If an older machine is used, the electrodes may be moved at different times during the test to measure your heart's electrical activity from different locations on your chest.

2.1. Risks
There is no chance of problems while having an electrocardiogram (EKG or ECG). An EKG is a completely safe test. In most cases, there is no reason why you should not be able to get an EKG.

The electrodes are used to transfer an image of the electrical activity of your heart to tracing on paper. No electricity passes through your body from the machine, and there is no danger of getting an electrical shock.

III. Introduction to ECG wave
The ECG is nothing but the recording of the hearts electrical activity. The deviations in the normal electrical patterns indicate various cardiac disorders. Cardiac cells, in the normal state are electrically polarized. Their inner sides are negatively charged relative to their outer sides. These cardiac cells can lose their normal negativity in a process called depolarization, which is the fundamental electrical activity of the heart. This depolarization is propagated from cell to cell, producing a wave of depolarization that can be transmitted across the entire heart. This wave of depolarization produces a flow of electric current and it can be detected by keeping the electrodes on the surface of the body. Once the depolarization is complete, the cardiac cells are able to restore their normal polarity by a process called re-polarization. This is also sensed by the electrodes. The earlier method of ECG signal analysis was based on time domain method. But this is not always sufficient to study all the features of ECG signals. So, the frequency representation of a signal is required. To accomplish this, FFT (Fast Fourier Transform) technique is applied. But the unavoidable limitation of this FFT is that the technique failed to provide the information regarding the exact location of frequency components in time. As the frequency content of the ECG varies in time, the need for an accurate description of the ECG frequency contents according to their location in time is essential. This justifies the use of time frequency representation in quantitative electro cardiology. The immediate tool available for this purpose is the Short Term Fourier Transform (STFT). With the development of digital signal processing technology, FIR filters are realized by single-chip, DSP, programmable logic devices. Compared to the FPGA, single-chip is not flexible enough, and the DSP can be flexible, although more slowly, so using FPGA realizing FIR digital filter has the characteristic of the real-time, high flexibility, faster processing speed and small volume production of low cost. At present, the digital filter signal processing in dealing with ECG occupy a larger location, the use of neural networks can achieve a good filtering effect, but need for a reference input, ECG signals cannot be updated at the same time, and in the hardware it is difficult to achieve in the MCU and DSP as the main controller, its filtering is completed in the hardware, which is a portable ECG monitoring has increased the burden of hardware circuits the former FPGA limited by internal resources, can only be limited to filter the 50Hz frequency interference. In view of this, the portable ECG monitor reduce the hardware circuits and get the better ECG signal, this paper proposes the use of both 50Hz in FPGA filtering and 0.05 ~ 100Hz band-pass filtering of the double filtering.

3.1 ECG Analysis
The ECG records the electrical activity of the heart, where each heart beat is displayed as a series of electrical waves characterized by peaks and valleys. Any ECG gives two kinds of information. One, the duration of the electrical wave crossing the heart which in turn decides whether the electrical activity is normal or slow or irregular and the second is the amount of electrical activity passing through the heart muscle which enables to find whether the parts of the heart are too large or overworked. Normally, the frequency range of an ECG signal is of 0.05–100 Hz and its dynamic range – of 1–10 mV. The ECG signal is characterized by five peaks and valleys labeled by the letters P, Q, R, S, T. In some cases we also use another peak called U.

The performance of ECG analyzing system depends mainly on the accurate and reliable detection of the QRS complex, as well as T- and P waves. The P-wave represents the activation of the upper chambers of the heart, the atria, while the QRS complex and T-wave represent the excitation of the ventricles or the lower chamber of the heart. The detection of the QRS complex is the most important task in automatic ECG signal analysis. Once the QRS complex has been identified a more detailed examination of ECG signal including the heart rate, the ST segment etc. can be
performed. In the normal sinus rhythm (normal state of the heart) the P-R interval is in the range of 0.12 to 0.2 seconds. The QRS interval is from 0.04 to 0.12 seconds. The Q-T interval is less than 0.42 seconds and the normal rate of the heart is from 60 to 100 beats per minute. So, from the recorded shape of the ECG, we can say whether the heart activity is normal or abnormal. The electrocardiogram is a graphic recording or display of the time variant voltages produced by the myocardium during the cardiac cycle. The P-, QRS- and T-waves reflect the rhythmic electrical depolarization and repolarization of the myocardium associated with the contractions of the atria and ventricles. This ECG is used clinically in diagnosing various abnormalities and conditions associated with the heart.

![Figure 1. The normal ECG waveform.](image)

The normal value of heart beat lies in the range of 60 to 100 beats/minute. A slower rate than this is called bradycardia (Slow heart) and a higher rate is called tachycardia (Fast heart). If the cycles are not evenly spaced, an arrhythmia may be indicated. If the P-R interval is greater than 0.2 seconds, it may suggest blockage of the AV node.

1) Certain disorders, involving heart valves cannot be diagnosed from ECG. Other diagnostic techniques such as angiography and echocardiography can provide information not available in ECG.

2) Each action potential in the heart originates near the top of the right atrium at a point called the pacemaker or sensorial (SA) node.

3) The wave generated by action potential, terminates at a point near the center of the heart, called the atrioventricular (AV) node.

The horizontal segment of this waveform preceding the P-wave is designated as the baseline or the isopotential line. The P-wave represents depolarization of the arterial musculature. The QRS complex is the combined result of the repolarization of the atria and depolarization of the ventricles, which occur almost simultaneously.

The T-wave is the wave of ventricular repolarization, where as the U-wave, if present is generally believed to be the result of after potentials in the ventricular muscle. So, the duration amplitude and morphology of the QRS complex is useful in diagnosing cardiac arrhythmias, conduction abnormalities, ventricular hypertrophy, myocardial infection and other disease states.

3.2 STFT

Channelization is used for finding the instantaneous parameters of the ECG signals; this approach allows reporting the instantaneous frequency of a signal. Channelization is one of the most important operations in building digital receivers. The equivalent analog operation is the filter bank. Therefore, digital channelization can be considered as a digital filter bank. It can also be considered as an N-port network with one input and N-1 outputs. An input signal will appear at a certain output according to its frequency. By measuring the outputs from the filter bank, the frequency of the input signal can be determined. The only practical approach to building a wideband digital receiver for signal intelligence applications with today's technology is through channelization. An efficient method of performing channelization is by employing the fast Fourier transform (FFT). To build a signal intelligence receiver using FFT, the length and the overlap of the FFT are very important parameters. These parameters are related to the minimum pulse width and the frequency resolution, which determines the sensitivity of the receiver. The frequency information can be obtained from the outputs of the digital filters. In order to obtain the input frequency, the filter outputs must be further processed. The main objectives of a receiver are to determine the number of input signals and their frequencies. The circuit used to accomplish these goals is referred to as the encoder. The encoding circuit is the most difficult subsystem to design a receiver. Most
research effort is spent on the encoder design. This is true for both digital and analog receivers. The main problems are to avoid the generation of false signals and the detection of weak signals. In an analog filter bank, the shape of the filter is difficult to control, and it is difficult to build filters with uniform performance such as the bandwidth and the ripple factor; therefore, the encoder must accommodate this problem. The shape of each individual filter in a digital filter bank can be better controlled. As a result, the encoder should be slightly easier to design because it does not need to compensate for the filter differences.

3.3 FILTERBANKS

The straightforward approach for building a filter bank is to build individual filters, each one with a specific center frequency and bandwidth. Figure 1 shows such an arrangement. Each digital filter can be either a finite impulse response (FIR) or infinite impulse response (IIR) type.

![Figure 1 A filter bank.](image)

Theoretically, each filter can be designed independently with a different bandwidth or shape. In this arrangement, if the input data are real (as opposed to being complex) the output data are also real. The output is obtained through convolving the input signal \( x(n) \) and the impulse response of the filter \( h(n) \). One of the disadvantages of this approach is that the operation of the filter bank is computationally complex. It is desirable to build a receiver with uniform frequency resolution; that is, the filters have the same shape and bandwidth. It is easier to build such a filter bank through FFT techniques than by using individual filter design because there is less computation.

3.4 FFT AND CONVOLUTION OPERATIONS

In the previous section, it is stated that the outputs of a filter bank can be obtained from convolution and also from the FFT operation. In this section the similarity between the FFT and convolution operation will be illustrated. In the FFT operation, one set of data in the time domain can be used to find one set of data in the frequency domain. In order to process the input data in a continuous manner, the FFT must also operate continuously.

Let us assume that one frequency component from the FFT output is equivalent to one filter output at a specific point in time from a filter bank. The output of the \( k \) component \( X(k) \) from an \( N \) point FFT can be written as

\[
X(k) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi kn/N}
\]

The \( k_0 \) component of \( X(k_0) \) can be written as

\[
X(k_0) = \sum_{n=0}^{N-1} x(n) e^{-j2\pi kn/N}
\]

In order to relate this output to convolution, let us define an impulse function as

\[
h(k) = e^{-j2\pi k_0 k/N}
\]

Where \( k = - (N-1), - (N-2) \ldots - 1, 0; \) then

\[
h(k - n) = e^{-j2\pi (k-n) k_0/N}
\]

If \( k = 0 \), then

\[
h(k - n)|_{k=0} = e^{-j2\pi k_0 n/N}
\]

Thus

\[
X(k_0) = \sum_{n=0}^{N-1} x(n) h(k - n)|_{k=0}
\]

One can see that this expression is a discrete convolution. It represents the input signal \( x(n) \) convolving with \( h(k - n) \). This operation illustrates that a certain frequency bin from the FFT operation can be treated as an input signal convolved with a certain impulse function. Therefore, one can consider that each individual FFT output can be represented by a filter impulse function convolved with the input signal. Because the FFT operation is rather simple compared with an individual filter design, the FFT will be used for filter bank design in the rest of this chapter.

3.5 OVERLAPPING INPUT DATA IN THE FFT OPERATION
In the previous section it was demonstrated that each FFT output can be considered as a filter output. In order to operate on a continuous input signal, the FFT must operate on different intervals of data at different times. Usually, the initial data point is labeled \( n = 0 \), and the data interval can slide \( M \) points and be represented by \( n = M \). The corresponding FFT can be written as

\[
X(k) = \sum_{n=0}^{N-1} x(n) e^{-\frac{j2\pi kn}{N}}
\]

The \( M \) value must be changed continuously with the input signal. This operation is sometimes referred to as the short time Fourier transform (STFT). Figure 2 is used to illustrate the input data overlapping condition. In this figure the FFT uses only 8 data points. When \( M = 0, 1, 2, \ldots \), as shown in Figure 2(a), the input data slide one point every time, which is referred to as the sliding FFT. For this case the data can be considered 100% overlapping. If the minimum pulse width is 8 data points long, this approach can always fill one of the FFT windows with the shortest pulse. The time of arrival (TOA) resolution is equal to the \( ts \), where \( ts \) is the sampling time and \( f_s \) the sampling frequency. With 100% overlapping, the FFT must be performed every \( ts \) seconds thus, the computation load is very high, to give best resolution possible. In this project an 8-point FFT with 100% overlapping (as shown in Figure 2(a)) is implemented.

(a) 

(b) 

(c) 

(d) 

Figure 2 Data samples in time domain: (a) 100% overlap, (b) 50% overlap, (c) zero overlap, and (d) missing of data.

IV. FPGA and TOOL FLOW

FPGA Design Considerations

FPGA demonstrates good performance and logic capacity by exploiting parallelism. At present single FPGA platform can play multi-functions, including control, filter and system. FPGA design flow is a three-step process consisting of design entry, implementation, and verification stages, as shown in Fig 3.1. The full design flow is an iterative process of entering, implementing, and verifying the design until it is correct and complete. The key advantage of VHDL when used for systems design is that it allows the behavior of the required system to be described (modeled) and verified (simulated) before Synthesis tools translate the design into real hardware (gates and wires). HDL describes hardware behavior. There are main differences between traditional programming languages and HDL. Traditional languages are a sequential process whereas

- HDL is a parallel process.
- HDL runs forever whereas traditional programming language will only run if directed.

Fig (2.1): FPGA design flow
FPGA Design and Programming Tool Flow
Fig (2.7): Xilinx Design Flow

The standard design flow comprises the following steps:
Design Entry and Synthesis: In this step of the design flow, a design is created using a hardware description language (HDL) for text-based entry. Xilinx Synthesis Technology (XST) GUI can be used to synthesize the HDL file into an NGC file.
Design Implementation: By implementing to a specific Xilinx architecture, the logical design file format, such as EDIF, that is created in the design entry and synthesis stage is converted into a physical file format. The physical information is contained in the native circuit description (NCD) file for FPGAs. Then a bit stream file is created from these files and optionally a PROM or EPROM is programmed for subsequent programming of Xilinx device.
Design Verification: Using a gate-level simulator or cable, it is ensured that the design meets timing requirements and functions properly.

Fig (2.8): Xilinx Spartan 3e FPGA Kit

V. IMPLEMENTATION OF BLOCK DIAGRAM

Figure 3.1 block diagram of ECG

Using Matlab heartbeat is generated that will be forced on sound card of the system; heartbeat signal will be given to the ADC to convert analog signal to 12 bit digital signal. Interfacing code will convert serial 12 bit data to parallel 12 bit that is feed to notch filter. ECG signal coefficients that are stored in the ROM are designed with help of Matlab. To select which input signal has to be accessed, can be selected by a sliding switch present on the FPGA board. Resultant signal is feed to Notch Filter. Notch filter is designed to operate at a frequency of 50 Hz (attenuation), in order to remove power supply interference noise. Data thus obtained from the Notch filter is sent to high frequency noise removal filter. This filter is designed to attenuate signals which are not in the range of 0.05 to 100 Hz (allows these frequencies only). The output from high frequency noise removal filter is given to block ram which store the data in it and forwards data to STFT (Short Time Fourier Transform) block to process FFT on the signal. STFT is developed by Xilinx IP core so Block ram is also embedded in the core which is utilized in the project. So external block ram is not required as shown in block diagram, STFT is used to analyze frequency response of the heartbeat. Magnitude and phase comparator module will carry out time domain analysis i.e. magnitude and time period of each wave (P, Q, R, S & T).

ADC Module

Analog input interface (ADC)

FPGAs are well suited for serial Analog to Digital (A/D) converters. This is mainly because serial interface consumes less communication lines while the FPGA is fast enough to accommodate the high speed serial data. The ADCS7476MSPS is a high speed, low power, 12-bit A/D converter. A/D converter is a high speed serial interface that interfaces easily to FPGAs. The A/D interface adapter (AD1_PMOD) is implemented within the FPGA. (Fig. 3.4). Inside the FPGA, this adapter facilitates parallel data acquisition. Sampling is initiated at the rising edge of a clock applied at the line sample. The timing diagram of the communication protocol obtained with Modelsim is illustrated in Fig. 3.5.

Figure 3.4 pmod connection diagrams
Figure 3.5 ADCS7476 Serial Interface Timing Diagram

When reset is given all the data in spdata2 shift register and counter count will be cleared. When clk is at raising edge counter will starts upward counting. If count is above ‘3’ and raising edge of clk is applied then input sdata2 (serial data) will be forced on to spdata2 shift register LSB. When count reaches “15” then data in shift register will be reflected parallel on to pdata2 that is a 12 bit bus. At that time cs will be active high signal. Pclk will be at active high signal for above count of ‘8’.

Coefficient Generation for Notch and High Pass Noise Removal Filter.

Notch filter and High Pass Noise Removal filter.
The filter coefficients are generated by mat lab by given process below
Start → Mat lab → toolboxes → filter design HDL coder → filter design and analysis tool (FDA tool).
Open FDA tool then select as shown An ECG signal is generated from mat lab by using the command ECG for a sampling rate of 160 as shown below because normal heartbeat rate is 72 beats per/min i.e. 0.83 sec for the beat so no of samples taken for the beats 160 samples as shown in the figure. A mat-lab code has been developed to convert data in the workspace to binary format according to specified length. The generated values in binary format is copied and saved in the ECG ROM. As the clk is given the values are given to the output which will result in ECG signal.

Synthsids report ECG Rom block

VI. SIMULATION RESULTS

CHIP SCOPE RESULTS:
VII. CONCLUSIONS
This paper introduces the ECG FIR filter design method based on FPGA, the results of high-frequency and 50Hz power-frequency interference dual filters can be seen, the filters can be used directly in FPGA embedded ECG monitor design, ECG monitor system to collect, store, playback, wireless transmission can be integrated into a FPGA chip, so that greatly reducing the development of analog circuits, reducing development costs and research and design cycle, the filters have a good application value.

REFERENCES


