Design Of Ternary Arithmetic Circuits Using QDGFET

Shah Jay  
Dept. of VLSI & Embedded System Design  
GTU PG School, Ahmedabad, India  
jayshah.0309@live.com

Prof. Satish Narkhede  
Dept. of Electronics & Tele Communication  
PICT, Pune, India  
ssn_pict@yahoo.com

Abstract—This paper presents a novel design of ternary arithmetic circuits like half-adder and multiplier using quantum dot field effect transistors. Due to the change in threshold voltage over the range QDGFETs produce one intermediate state between two normal stable ON and OFF states. Moreover ternary logic is a promising alternative to the conventional binary logic design technique, since it is possible to produce three states (FALSE, UNKNOWN, TRUE), and also reduces the number of interconnects and chip area and increases efficiency. In this paper we have proposed novel circuit design of half-adder and multiplier based on ternary logic QDGFETs. Increased number of states in QDGFETs will increases the number of bit handling capacity in the device.

Keywords—Quantum Dot Field Effect Transistor (QDGFET), MVL(multi valued logic), Half-Adder, multiplier.

I. INTRODUCTION

The basic building block of any electronic circuit is the metal-oxide semiconductor field effect transistor (MOSFET). The current flow from the source to drain region of a MOSFET is controlled by the applied voltage in its gate terminal. Semiconductor industries are always trying to decrease the feature size of MOSFET. Over the past 30 years, when a new technology node is introduced every 2–3 years, the number of transistors per chip has doubled which was first predicted by Gordon Moore in 1965 and is commonly referred to as Moore’s law. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area.

The speed of a MOSFET is increased and the power consumption is also decreased when the feature size of a MOSFET is decreased. But when the feature size starts to approach sub-22 nm, several issues begin to make further minimization difficult [1-2]. As transistors have decreased in size, the thickness of the gate dielectric needs to decrease [3-4]. When the gate dielectric thickness scales down below 2 nm, leakage currents due to the tunneling of charge carriers increase drastically. The tunneling of charge carriers increases the power consumption and reduces device reliability. Another problem is sub-threshold conduction of the MOSFET. Because of the nm range channel length, the source to drain leakage of the current decreases the on and off current ratio of the device and destroys its switching property. Process variations are also a major issue in the sub-22 nm range.

Traditionally, digital computation is performed on two-valued logic, i.e., there are only two possible values (0 or 1, true or false) in the Boolean space. Multiple-valued logic (MVL) replaces the classical Boolean characterization of variables with either finitely or infinitely many values such as ternary logic [5] or fuzzy logic [6]. Ternary logic (or three-valued logic) has attracted considerable interest due to its potential advantages over binary logic for designing digital systems.

Multivalued logic (MVL) has the following advantages.

1) In MVL, each wire can transmit more MVL information than a binary element. As a result, the number of connections inside the chip can be reduced.

2) Since each MVL element can process more information than a binary element, the complexity of circuits may be decreased.

3) The ON- and OFF-chip connections can be reduced to help alleviate the pin-out difficulties that arise with increasingly larger chips.

4) The speed of serial information transmission will be faster since the transmitted information per unit time is increased.

However, MLV circuits have static power dissipation problem [7].

A conventional MOSFET can handle two bits because of its two states: ON and OFF. They are suitable for binary implementation. Research is ongoing towards the development of devices that are suitable for multi-valued operation. All the devices that have been proposed so far to implement MVL, have more serious problems than complementary MOS
CMOS), such as excess leakage current, being unable to operate at room temperature or requiring complex fabrication processes. [8] One major problem of the band-to-band tunneling mechanism is the leakage current which reduces both the ON-OFF current ratio of the device and the noise margin.

However, in a quantum dot gate field effect transistor (QDGFET), direct tunneling occurs through the tunnel insulator, and the quantum dots act as charge storage elements. The generated intermediate state is more stable in a QDGFET because of the reduced charge leakage through the cladding of the QDs in the gate region. Thus, QDGFETs provide the capability to process multiple bits in a single device and provide higher levels of bit density without further feature size minimization. Besides this QDGFET can be fabricated using conventional CMOS process technology. The integration problem for other devices with existing CMOS technology can be solved in QDGFETs.

This paper is organized as follows. Section II give us a brief introduction of Quantum dot gate field effect transistors, followed by the review of ternary logic in Section III. Arithmetic Logic Circuits are then proposed, analyzed, and evaluated with respect to its functional operations and Simulation results are shown in Section IV, which is followed by conclusion in Section V.

II. QUANTUM DOT GATE FIELD EFFECT TRANSISTOR

Quantum dots are some miniature structures of a single atom or number of atoms. Quantum dots almost behave like a single atom because of three dimensional confinement of electron wave function inside the dots.

In QDGFET, two layers of QGs are deposited on top of the gate insulator. The presence of QDs in the gate region of the FET produces three states in their transfer characteristics. The device structure of a QDGFET is shown in Fig. 1. This FET produces its characteristics at room temperature. They can be fabricated by using conventional CMOS process technology. QDs are fabricated by using site specific self-assembly process [9-10].

QDs deposited in the gate region have silicon (Si) or germanium (Ge) nanocrystal surrounded by their oxide. The presence of tunnel oxide surrounding the semiconductor nanocrystal, decreases the charge leakage from individual QDs. The three state behaviour of QDGFET depends on the charge storage property of the QDs in the gate region. Because of surrounding tunnel oxide, charge leakage from one QD doesn’t affect the charge leakage from another QD. Besides this, another improved structure which increases the stability of the device characteristics is introduced elsewhere [11-12].

A. Device Structure:

Figure 1 show the device structure and the cross – sectional schematic of a QDGFET, respectively. Two layers of SiOx-cladded Si quantum dots are self-assembled on the lattice matched multi stack gate insulator layer.

The doping concentration of a p-type substrate is \( N_A = 5 \times 10^{16} \text{cm}^{-3} \). The gate length is 0.5 m. The oxide thickness and device width are 20 nm and 20 m, respectively. The source and drain doping concentration is \( N_D = 10^{20} \text{cm}^{-3} \). The width of the source and drain region is 1 m. The depth of the source and drain region is 0.25 m. The depth of the substrate is 100 m. Intrinsic carrier concentration (\( n_i \)) is 1.5 \times 10^{10} \text{cm}^{-3}. The mobility of a electron (\( \mu \)) in Si is considered as 500 cm\( ^2 \) V\( ^{-1} \)Sec\( ^{-1} \). The modeling is considered for room temperature which gives \( kT/q \) = 0.026 V.

![Figure 1 Cross-sectional schematic of a quantum dot gate field-effect](image)

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B. Theory of Operations:

The drain current of a QDGFET can be expressed as in (1)

\[
I_D = \frac{W}{2L} C_{ox} \mu_n \left[ \left( V_D - V_T \right) V_2 - \frac{V^2_D}{2} \right] \tag{1}
\]

The intermediate state generates because when the gate voltage (VG) of the device is increased, the threshold voltage (VTH) of the device also increases because of resonant tunneling of charge carriers from the inversion channel to different layers of quantum dots in the gate region, which makes \( (V_G - V_{TH}) \) constant in (1).

The tunneling rate \( P \) is responsible for transfer of charge from the channel to the QD layers. The charge on a dot in a layer is calculated by determining the tunneling rate of transition. The tunneling transition rate from the channel to the two quantum dot layers is expressed by Hamiltonian in Eq.2 [14-15].

\[
P_d = \frac{4 \pi}{h} \sum_{\omega \Delta \omega} \left| \langle \psi_{\omega} | H_1 | \psi_{\omega} \rangle \right|^2 (f_{\omega} - f_{\Delta \omega}) \delta (E_{\omega} - E_d).
\]

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The charge in the gate region due to quantum dots is discrete as expressed by Eq. 3. The variation in flat band voltage \( V_{FB} \) due to the charged state of quantum dots in the gate results in corresponding change in the threshold voltage \( \Delta V_{TH} \). The variation in the value of charge on the two QD layers, as the \( V_g \) is increases, causes change in the threshold voltage expressed in Eq. 3.

\[
\Delta V_{TH} = \frac{q}{\sum_{x} \sum_{y} \Delta V_{qD1} \Delta V_{qD2}} \left( \frac{V_{GS}}{V_{GS0}} \right)
\]

(3)

Here, \( X_{QD1} \) and \( X_{QD2} \) are the distances of quantum dot cores from the gate contact, \( n_1 \) and \( n_2 \) are the number of dots in layer 1 and 2, respectively, \( N_{QD1} \) and \( N_{QD2} \) are the charge on each SiOx-cladded Si quantum dots, \( C_{ox} \) is the oxide capacitance (which is modified due to the presence of quantum dots). In addition, \( x_g \) is the distance of the Si-SiOx interface from the gate, \( \rho \) is the charge density and \( q \) is the electron charge.

C. QDGFT Circuit Model:

The effective threshold voltage is divided into three regions, OFF state, Intermediate state, and ON state, depending on its transfer characteristics. The threshold voltage changes linearly with respect to gate voltage when it increases from \( V_{GE1} \) to \( V_{GE2} \). The change is controlled by the \( q \) parameter.

\[
V_{T_{eff}} = \begin{cases} V_{T} & V_{GS} < V_{GE1} \\ V_{T} + \alpha (V_{GS} - V_{GE1}) & V_{GE1} < V_{GS} < V_{GE2} \\ V_{T} + \alpha (V_{GS} - V_{GE2}) & V_{GS} < V_{GE2} \end{cases}
\]

(4)

Using the equations for \( V_{T_{eff}} \) from equation 4, the drain current equation can be derived using traditional MOSFET circuit modeling techniques.

\[
I_{DS} = \begin{cases} 0 & V_{GS} < V_{T_{eff}} \\ \frac{W}{L} C_{ox} \alpha (V_{GS} - V_{T_{eff}}) V_{DS} & V_{DS} < V_{GS} < V_{T_{eff}} \\ \frac{W}{L} C_{ox} \left( V_{GS} - V_{T_{eff}} \right)^2 & V_{DS} > V_{GS} - V_{T_{eff}} \end{cases}
\]

(5)

We have used Berkeley Simulation Model (BSIM 3.2.0 and BSIM 3.2.4) and conducted simulations of QDGFTs based arithmetic circuits using H-Spice.

III TERNARY LOGIC

The binary logic when given a significant third value becomes ternary logic and the functions realized with the three values are called as Ternary logic functions. The values 0, 1 and 2 form the nomenclature to denote the ternary values in this paper. A function \( f(X) \) is defined as a ternary logic function mapping \( f(0, 1, 2) \) to \( f(0, 1, 2) \), where \( X = \{X1, \ldots, Xn\} \). When \( X_i, X_j = \{0, 1, 2\} \) [13], the basic operations of ternary logic can be defined as follows.

\[
X_i + X_j = \max \{X_i, X_j\}
\]

\[
X_i \cdot X_j = \min \{X_i, X_j\}
\]

(6)

Where \( - \) denotes the arithmetic subtraction, the operations +, \( \cdot \), and are referred to as the OR, AND, and NOT operations respectively for ternary logic.

The logic symbols for different levels assumed are shown in Table I. A general ternary inverter operates with one input and three outputs. The logic symbols for different levels assumed are shown in Table I. A general ternary inverter is an operator with one input and three outputs. The Table II shows the ternary inverter, where \( x \) is input and \( y_0, y_1 \) and \( y_2 \) are the outputs. To generate the outputs \( y_0, y_1 \) and \( y_2 \) the three inverters that are needed are standard ternary inverter (STI), positive ternary inverter (PTI) and a negative ternary inverter (NTI) respectively. The ternary circuits are designed according to the convention defined by (6).

<table>
<thead>
<tr>
<th>Voltage level</th>
<th>Logic Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>½ Vdd</td>
<td>1</td>
</tr>
<tr>
<td>Vdd</td>
<td>2</td>
</tr>
</tbody>
</table>

TABLE II TRUTH TABLE OF TERNARY INVERTERS

<table>
<thead>
<tr>
<th>Input (x)</th>
<th>STI (y_0)</th>
<th>PTI (y_1)</th>
<th>NTI (y_2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

IV. ARITHMETIC CIRCUIT USING QDGFT

A. 1-BIT MULTIPLIER:

In ternary 1-bit multiplier two ternary bit are multiplied with each other out of which one is product bit and one is carry bit. The karnaugh map of the 1-bit multiplier is shown in table III (A and B). The block diagram and the input output waveform is shown in Fig (3) and (4) respectively.

<table>
<thead>
<tr>
<th>A/B</th>
<th>0</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

TABLE III KARNAUGH MAP (A) PRODUCT (B) CARRY OF 1-BIT MULTIPLIER
Solving the above karnaugh Table we get the simplified Boolean equation of product and carry as in Eq.7. Here A0 represents the low state, A1 represents the intermediate state, and A2 represents the high state.

Product = \((A_1B_2 + A_2B_1) + 1 \cdot (A_1B_1 + A_2B_2)\)

Carry = \(1 \cdot (A_2B_2)\) (7)

The Schematic circuit diagram of a ternary half-adder is shown in Fig. 2 which consists of ternary decoders, ternary AND gates and OR gates.

In the given block diagram we uses T-buffer which acts as a level shifter. It shifts higher level voltage (2) to middle level voltage (1). The logic function of a T-buffer can be represented as Eq. 8

\[ T = \begin{cases} 1, & \text{if input} = 1, 2 \\ 0, & \text{if input} = 0 \end{cases} \] (8)

The output from the decoder is passed through the ternary logic AND gates to generate different multiplied terms. Then two-input ternary OR gates are used to produce the sum-of-product (SOP) term. The final output of the product is generated by the OR gate which has two SOP input terms, out of which one passes through T-gate and other one from the previous OR gate.

<table>
<thead>
<tr>
<th>(A)</th>
<th>(B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
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<tr>
<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

The Schematic circuit diagram of a ternary half-adder is shown in Fig. 3 which consists of ternary decoders, ternary AND gates and OR gates. The circuit follow the same concept as discussed in 1-bit half adder.

<table>
<thead>
<tr>
<th>(A)</th>
<th>(B)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

B. HALF-ADDER:

In ternary half-adder two ternary bit are added with each other out of which one is sum bit and one is carry bit. The karnaugh map of the half-adder is shown in table IV (A and B). The block diagram and the input output waveform is shown in Fig. 3 and 5 respectively.

Solving the above karnaugh Table we get the simplified Boolean equation of product and carry as in Eq. 9. Where \(A_k\) and \(B_k\) are the outputs from the decoder corresponding to the \(A\) and \(B\) input shown in Fig. 3

\[
\text{Sum} = A_2B_0 + A_1B_1 + A_2B_2 + 1 \cdot (A_1B_0 + A_2B_1 + A_2B_2) \\
\text{Carry} = 1 \cdot (A_2B_1 + A_2B_2 + A_1B_2) \] (9)

The Schematic circuit diagram of a ternary half-adder is shown in Fig. 3 which consists of ternary decoders, ternary AND gates and OR gates. The circuit follow the same concept as discussed in 1-bit half adder.

![Figure 2: Block diagram of ternary 1-bit multiplier](image)

![Figure 3: Block diagram of ternary Half-Adder](image)

V. SIMULATION
VI. CONCLUSION

This paper presented the design of a novel ternary logic arithmetic circuits based on quantum dot field effect transistors (QDGFET). Less power dissipation was observed in the QDGFET-based ternary logic circuits than the other. The improved performance of QDGFET-based ternary logic circuits was because of the fast resonant tunneling mechanism of the charge carrier from the inversion channel to the different layers of quantum dots in the gate region. Thus making the QDGFET a promising circuit element in MVL circuits in the near future.

REFERENCES